Notice of Allowability	Application No.	Applicant(s)	
	09/740,113	SEITZ ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☒ The drawings filed on *19 December 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 09/22/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-18 are allowed.

2. The following is a statement of reasons for the indication of allowable subject matter:

Claims 1 and 3, recite, inter alia, "*a method of forming in a semiconductor body which comprises an array of memory cells, each memory cell comprises an insulated gate field effect transistor having a gate which is separated from the semiconductor body by a gate dielectric layer, the method comprising the steps of: forming first insulating regions around portions of the top surface of the semiconductor body and surround the gate contacts; forming second insulating regions around exposed portions of the gate contacts; and forming a borderless contact to each one of the first output regions of each transistor with the first and second insulating regions electrically isolating the gate contacts from the contacts to the first output regions*"; in the combination with other claimed features.

Claims 5, 6 and 14, recite, inter alia, "*a method of forming in a semiconductor body which comprises an array of memory cells, each memory cell comprises a trench capacitor and a vertical insulated gate field effect transistor having a gate which is separated from a vertical surface of the semiconductor body by a gate dielectric layer, the method comprising the steps of: forming a first insulating layer over a top surface of the semiconductor body; over filling the first openings through the first insulating layer with a first conductor which contacts the gates of each transistor and extends over a top surface of the first insulating layer; forming first openings through the second insulating layer and second openings through the first insulating layer between adjacent insulating sidewall spacer regions to expose portions of the semiconductor top*

surface which include portions of the first output regions; and filling each of the second openings through the first insulating layer with a second conductor which contacts a first output region such that each second conductor is self aligned and borderless"; in the combination with other claimed features.

3. The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

4. Mandelman et al (U.S. 6,288,422) teaches a structure and its process for fabricating a DRAM cell having MOSFET and large trench capacitance, Aoki et al (U.S. 6,744,104) teaches Semiconductor integrated circuit including insulated gate field effect transistor and method of manufacturing the same, and Hsiao et al (U.S. 6,391,705) teaches Fabrication method of high-density semiconductor memory cell structure having a trench, they do not teach the above-mentioned limitations.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on Monday through Thursday and on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TYT

David A. Zarneke
Primary Exam
6/22/04